REMARKS

The Office Action mailed on November 14, 2006 has been received and its contents carefully considered.

The present Amendment revises claims 1, 12, 14, 20, and 32-34. It is respectfully submitted that the pending claims 1-6, 12-19, 20-27, and 32-34 patently define over the prior art, and that the rejection of the claims should be withdrawn in view of the revisions to the claims.

Regarding The Indefiniteness Rejection

Claim 14 is rejected under 35 U.S.C. §112, second paragraph, as being indefinite, as set forth in page 2 of the Office Action. In response, claim 14 has been amended. Thus, withdrawal of the rejection is respectfully requested.

Regarding The Anticipation Rejection

Claims 12, 15-17, 20, 22, and 27 stand rejected under 35 U.S.C. §102(e) as anticipated by U.S. patent 6,216,224 to Klein. Among the claims being rejected for anticipation, claims 12 and 20 are independent. It is respectfully submitted that claims 12 and 20 are patentable over Klein for the reasons noted below.

Claim 12, as amended, recites:

> A method for accessing initialization data for starting up a central processor unit in a computer system that also includes a bus, a south-bridge chip connected to the bus, and a north-bridge chip connected between the bus and the central processor unit, the method comprising:
>
> **providing a non-volatile memory connected to the south-bridge chip, wherein the non-volatile memory includes a first memory space storing routines and code of a basic input/output system (BIOS) and a second memory space storing**

initialization data, and wherein the initialization data is excluded from the BIOS and is used for initialization of the central processor unit;

(a) sending a request from the north-bridge chip to the south-bridge chip in order to access the initialization data from the non-volatile memory;

(b) **in response to the request, accessing the second memory space of the non-volatile memory to read out the initialization data by the south-bridge chip;**

(c) sending the initialization data from the south-bridge chip to the north-bridge chip; and

(d) **activating the central processor unit by receiving the initialization data sent from the south-bridge chip and then setting initial values for initialization of the central processor unit based on the initialization data received by the north-bridge chip from the south-bridge chip, wherein no random access memory is used to store said initialization data during step (d).** (Emphasis added).

Applicants respectfully submit that claim 12, as amended, patently defines over Klein for at least the reason that Klein fails to disclose or suggest the features emphasized above.

In rejecting claim 12, the Office Action relies on Klein's use of read-only memory (ROM) shadowing, a process performing during booting of a computer system for transferring firmware routines from a ROM to a RAM before CPU initialization (see column 1, lines 13-44; column 2, lines 1-18; column 4, lines 7-17; and column 4, lines 61-64). In particular, the Office Action relies on a few passages of Klein (e.g. lines 5-10, 20-35 of column 1, lines 1-20 of column 2, lines 25-30, 55-57 of column 3) and Figure 1 showing the path of transferring firmware routines of the BIOS from ROM 104 to RAM 118 to reject the claim, and all of the cited passages relate to ROM shadowing and require writing the firmware routines of the BIOS to the RAM 118.

The Office Action asserts that Klein (at column 2, lines 1-20) teaches activating the central processor unit for initialization of the CPU based on the initialization data received by the

north-bridge chip from the south-bridge chip. However, Klein fails to teach or even suggest that "**no random access memory is used to store said initialization data during step (d)**" or that "**the initialization data is excluded from the BIOS and is used for initialization of the central processor unit,**" as claim 12 now requires. The marked contrast between ROM shadowing as disclosure in Klein and claim 12 will be clearer from the following discussion.

In contrast to claim 12, Klein's "BACKGROUND OF THE INVENTION" section mentions (at column 1, line 62 to column 2, line 18, with emphasis added).

> FIG. 1 is a block diagram of the basic components of currently-available PCs that are involved in ROM shadowing. The firmware routines are stored as ROM data 102 in a ROM 104. During conventional ROM shadowing, the firmware routines are transferred, under control of the CPU 106, via an ISA bus 108, an ISA-20 PCI bus bridge 110, and a PCI bus 112 to a system controller 114. The system controller 114 then stores the data 116 in the RAM 118 via a memory bus 120. The CPU 106 repeatedly fetches and executes a small number of instructions from the ROM 104 via the ISA bus 108, the ISA-PCI bus bridge 110, the PCI bus 112, the system controller 114, and a CPU bus 122 in order to drive the system controller 114 to transfer the ROM data 102 to the RAM 118. When transfer of the firmware routines is complete, the CPU 106 is then initialized and, following initialization, the CPU fetches and executes the firmware initialization and BIOS routines directly from the system RAM 118 via the memory bus 120, system controller 114, and CPU bus 122. These routines direct the CPU 106 to read the operating system of the PC, or portions thereof, into the RAM 118 from a storage device (not shown), initialize various hardware and software system components (not shown), and thereby bring the PC up to a state where it can be used by a human operator.

In particular, Klein teaches that the firmware routines transferred to the RAM when a PC is booted include the routines of the basic input/output system ("BIOS") (see column 1, lines 28-30). It is noted that during conventional ROM shadowing, firmware routines are stored as ROM data 102 in a ROM 104 and the firmware routines (relied on by the Office Action as initialization

data) are transferred, under control of the CPU 106, via an ISA bus 108, an ISA-PCI bus bridge 110 (relied on by the Office Action as south bridge), and a PCI bus 112 to a system controller 114. The system controller 114 (relied on by the Office Action as a north bridge) then stores the data 116 in the RAM 118 via a memory bus 120.

In contrast, Klein does not teach or suggest "initialization data," as claim 12 requires. Claim 12 now requires that **the initialization data is excluded from the BIOS and is used for setting initial values for initialization of the central processor unit.** Klein fails to teach or suggest these features relating to "initialization data."

Since Klein teaches ROM shadowing, what Klein actually discloses is that upon receiving the data of the firmware routines that are sent by the ISA-PCI bus bridge 110, the system controller 114 then stores the data 116 in the RAM 118 (see column 2, lines 1-3). In addition, regarding conventional ROM shadowing, the CPU 106 repeatedly fetches and executes a small number of instructions from the ROM 104 via the ISA bus 108, the ISA-PCI bus bridge 110, the PCI bus 112, the system controller 114, and a CPU bus 122 in order to drive the system controller 114 to transfer the ROM data 102 to the RAM 118 (see column 2, lines 6-18).

Klein fails to teach or suggest step (d) of claim 12. Step (d) now requires "activating the central processor unit by receiving the initialization data sent from the south-bridge chip and then setting initial values for initialization of the central processor unit based on the initialization data received by the north-bridge chip from the south-bridge chip, wherein no random access memory is used to store said initialization data during step (d)" (emphasis added).

For at least the above reasons, it is respectfully submitted Klein does not anticipate claim 12. Further, since Klein discloses a ROM shadowing method, Klein would have provided no suggestion or motivation to one of ordinary skill in the art at the time of the invention to change

the principle of ROM shadowing to transfer firmware routines from a ROM to a RAM in order to arrive at the invention now defined by claim 12. Therefore, it is respectfully submitted that independent claims 12, as well as its dependent claims 15-17, is neither anticipated nor rendered obvious by Klein, and the rejection of these claims be withdrawn.

Independent claim 20, as amended, recites:

> A system for accessing initialization data for starting a central processor unit, the system comprising:
>
> **a non-volatile memory including: a first memory space storing routines and code of a basic input/output system (BIOS) and a second memory space storing the initialization data, wherein the initialization data is excluded from the BIOS and is used for initialization of the central processor unit;**
>
> a south-bridge chip in direct communication with the non-volatile memory, **the south-bridge chip, when requested for the initialization data, accessing the initialization data from the second memory space of the non-volatile memory;**
>
> **a north-bridge chip**, coupled between the south-bridge chip and the central processor unit, **the north-bridge chip, when activated, sending a request for the initialization data to the south-bridge chip;**
>
> wherein **in response to the request from the north-bridge chip for obtaining the initialization data, the south-bridge chip accesses the initialization data from the second memory space and forwards the initialization data to the north-bridge chip for activating the central processor unit;**
>
> wherein **in response to the initialization data sent from the south-bridge chip, the north-bridge chip sets initial values for initialization of the central processor unit based on the received initialization data from the south-bridge chip in order to activate the central processor unit without using any random access memory to store the initialization data.**

Applicants respectfully submit that claim 20, as amended, patently defines over the cited reference for at least the reason that the cited reference fails to disclose the features emphasized above.

The apparatus defined by claim 20 includes features similar to those required by claim 12. Consistent with the above discussion as to patentability of claim 12, claim 20 is neither anticipated nor rendered obvious by Klein. In particular, as above mentioned, during conventional ROM shadowing, the firmware routines (relied on by the Office Action as initialization data) are transferred, under control of the CPU 106, via an ISA bus 108, an ISA-PCI bus bridge 110 (relied on by the Office Action as a south bridge), and a PCI bus 112 to a system controller 114. The system controller 114 (relied on by the Office Action as a north bridge) then stores the data 116 in the RAM 118 via a memory bus 120. (See column 1, line 65 to column 2, line 3).

In contrast, Klein fails to disclose or suggest the north-bridge chip, as required by claim 20, wherein **in response to the initialization data sent from the south-bridge chip, the north-bridge chip sets initial values for initialization of the central processor unit based on the received initialization data from the south-bridge chip in order to activate the central processor unit without using any random access memory to store the initialization data.** For at least the above reasons, it is respectfully submitted that claim 20, as well as its dependent claims 22 and 27, is neither anticipated nor rendered obvious by Klein. It is respectfully submitted that rejection of claims 20, 22, and 27 should be withdrawn.

Regarding The Obviousness Rejection

Claims 1-6, and 32 stand rejected under 35 U.S.C. §103(a) as being unpatentable over applicant's admission of prior art, in view of Klein. Claim 1 now recites:

> A method for accessing initialization data for starting up a central processor unit in a computer system comprising:
>
> **providing a non-volatile memory connected to a south-bridge chip, wherein the non-volatile memory includes a first memory space storing routines and code of a basic input/output system (BIOS) and a second memory space storing initialization data, and the initialization data is excluded from the BIOS and is used for initialization of the central processor unit;**
>
> (a) starting up a north-bridge chip that is coupled between the central processor unit and the south-bridge chip;
>
> (b) sending a request from said north-bridge chip to the south-bridge chip in order to access the initialization data from the second memory space of the non-volatile memory;
>
> **(c) starting up the central processor unit by receiving said initialization data from the south-bridge chip and then setting initial values for initialization of the central processor unit based on the received initialization data**, wherein **no random access memory is used to store said initialization data during step (c).**

It is respectfully submitted that claim 1, as amended, patently defines over the cited art for at least the reason that the cited art fails to disclose the features emphasized above.

In rejecting claim 1, the Office Action acknowledges that the AAPA does not teach "requesting initialization data from a south bridge chip" or that a "non-volatile memory stores BIOS and the initialization data." To resolve the deficiency of the AAPA, the Office Action asserts that various passages selected from Klein disclose limitations recited in claim 1. In particular, the selected passages include a passage at **column 2, lines 1-20**, which allegedly discloses starting up the CPU for initialization of the CPU based on the received initialization

data upon receiving said initialization data from the south bridge chip by said north-said chip. In addition, the passage at **lines 25-30 of column 3** is relied on by the Office Action as disclosing that the system controller 114 **transfers ROM data 102 to RAM 118**. Further, the Office Action asserts that "[I]t would be obvious to one [having] ordinary skill in the art to combine the teachings of Klein and applicant's admission of prior art" and that one having "ordinary skill in the art would have been motivated to request initialization data of CPU from a South Bridge chip as disclosed in Klein, since it would make the system compact as only one shared non-volatile memory for BIOS and initialization data is required, which is accessed by CPU through South Bridge."

Applicants respectfully disagree with the assertions set forth by the Office Action for the following reasons.

First, the AAPA does not teach "**providing a non-volatile memory connected to a south-bridge chip, wherein the non-volatile memory includes a first memory space storing routines and code of a basic input/output system (BIOS) and a second memory space storing initialization data, and wherein the initialization data is excluded from the BIOS and is used for initialization of the central processor unit**" and "**(c) starting up the central processor unit by receiving said initialization data from the south-bridge chip and then setting initial values for initialization of the central processor unit based on the received initialization data**, wherein **no random access memory is used to store said initialization data during step (c)**" as claim 1 now requires. In contrast, what the AAPA actually says is that "a serial PROM 200 is connected to the north bridge 204 by two input/output ports 202 of the north bridge 204" and that "[a]fter the north bridge 204 has started up, it sends a clock-like signal

to the serial PROM 200 and then reads the initialization data stored in the serial PROM 200" (see paragraph [0007]).

Second, these features missing from the AAPA are similar to those recited in claims 12 and 20. As to the above discussions as to the patentability of claim 12 indicate, the passages at Klein's column 2, lines 2-20 and column 3, lines 25-30 fail to teach or suggest the features that are missing from the AAPA. Thus, Klein does not disclose or suggest these features as required by claim 1.

Therefore, it is respectfully submitted that claim 1, as well as claims 2-6, is patentable over the prior art, and that the rejection should be withdrawn.

Applicants further provide the following additional reasons supporting the patentability of claim 1 as well as its dependent claims.

In determining obviousness, it is impermissible to pick and choose from any one reference only so much as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art.

It is respectfully submitted that neither the AAPA nor Klein suggests the combination proposed by the Office Action. The Office Action asserts that the motivation for the proposed modification to one of ordinary skill in the art is "since it would make the system compact as only one shared non-volatile memory for BIOS and initialization data is required, which is accessed by CPU through South Bridge." However, this reasoning for the proposed modification is a conclusory statement, not found in either the AAPA or Klein, and is not sufficient to establish a prima facie case of obviousness.

Klein discloses conventional ROM shadowing and also a method for ROM shadowing that is significantly different (see Klein's column 4, lines 24-46). Klein explains that

conventional ROM shadowing requires the CPU to repeatedly fetch and execute the code from the ROM, but Klein's method for ROM shadowing employs additional hardware, a ROM shadowing circuit (RSC), to drive the system controller to perform **transfer of the firmware routines from a ROM to a RAM and the CPU** is set to a reset state during the ROM shadowing.

Claim 1 requires that "**no random access memory is used to store said initialization data during step (d)**" and "**the initialization data is excluded from the BIOS and is used for initialization of the central processor unit.**" Since Klein sets forth ROM shadowing methods requiring transfer of routines from a ROM to a RAM, Klein would have provided no suggestion or motivation to one of ordinary skill in the art at the time of the invention to exclude essential features like storing firmware routines from a ROM to a RAM from Klein's teaching. That is, the reference would have provided no suggestion or motivation to change the principle of ROM shadowing that transfers firmware routines from a ROM to a RAM, in order to arrive to claim 1. In addition, since the AAPA states that "a serial PROM 200 is connected to the north bridge 204 by two input/output ports 202 of the north bridge 204" (see paragraph [0007] of the present application), the AAPA provides no suggestion or motivation to pick and choose different features from the conventional ROM shadowing method and the ROM shadowing method disclosed by Klein, remove necessary features relating to transfer of the firmware routines from the ROM to the RAM, and to combine these selected features into the AAPA but excluding the serial PROM 200 in order to arrive at all features of claim 1. That is, the principle operation of the AAPA and Klein would be changed greatly in the combination of the AAPA and Klein proposed in the Office Action.

MPEP section 2143.01 says that **"[I]f the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious."** Furthermore, MPEP section 2143 also advises that **"[t]he the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure."**

It is respectfully submitted that the argument in the Office Action is a classic example of impermissible hindsight reasoning. The Office Action has pointed to ***no teaching within the prior art that relates the desirability of combining the selected features***. As discussed above, it is the prior art which must properly suggest the desirability of combining the particular elements, for it is axiomatic that all elements and features are taught somewhere in the prior art. Thus, for at least these reasons, as a matter of law, the rejections of claims 1-6 are improper and should be withdrawn.

Claim 32 depends from independent claim 1, as amended. Consistent with the above discussion as to the patentability of claim 1, it is respectfully that claim 32 is not rendered obvious by the AAPA in view of Klein and that the rejection should be withdrawn.

Claims 13-14, 18-19, 21, 23-26, and 33-34 also stand rejected under 35 U.S.C. §103(a) as being unpatentable over Klein, in view of applicant's admission of prior art (AAPA). Applicants again respectfully disagree.

Claims 13-14 and 18-19 depend from independent claim 12, as amended. In addition, claim 12 includes features similar to those recited in claim 1. Consistent with the above discussion as to the patentability of claims 1 and 12, it is respectfully that claim 12 is patentable over the AAPA and Klein. In rejecting claims 13-14 and 18-19, no convincing suggestion or

motivation has been advanced as to why one of ordinary skill in the art at the time of the invention would have been motivated to modify or combine Klein with the AAPA so as to arrive at all features required by the rejected claims. In particular, the proposed combination fails to disclose or suggest that "**no random access memory is used to store said initialization data during step (d)**" and "**the initialization data is excluded from the BIOS and is used for initialization of the central processor unit,**" as required by claim 12. For at least this reason, it is respectfully submitted that claims 13-14 and 18-19 patently define over Klein in view of the AAPA, and that the rejection of these claims should be withdrawn.

Claims 21 and 23-26 depend from independent claim 20, as amended. Claim 20 includes features similar to those recited in claim 1. Consistent with the above discussion as to the patentability of claims 1 and 20, it is respectfully that claim 20 is patentable over the AAPA and Klein. In rejecting claims 21, 23-26, no convincing suggestion or motivation has been advanced as to why one of ordinary skill in the art at the time of the invention would have been motivated to modify or combine Klein and the AAPA so as to arrive at all features required by the rejected claims. In particular, the proposed combination fails to disclose or suggest that "**in response to the initialization data sent from the south-bridge chip, the north-bridge chip sets initial values for initialization of the central processor unit based on the received initialization data from the south-bridge chip in order to activate the central processor unit without using any random access memory to store the initialization data**" and "**a non-volatile memory including: a first memory space storing routines and code of a basic input/output system (BIOS) and a second memory space storing the initialization data, wherein the initialization data is excluded from the BIOS and is used for initialization of the central processor unit,**" as required by claim 20. For at least this reason, it is respectfully submitted

that claims 21 and 23-26 patently define over Klein in view of the AAPA, and that the rejection of these claims should be withdrawn.

Regarding claims 33-34, the Office Action acknowledges that "Klein does not teach setting initial values for initialization of the CPU based on received initialization data received by the North bridge." However, the Office Action asserts that "AAPA teaches setting initialization values for initialization using the initialization data sent by the north bridge." The Office Action then concludes that "[I]t would have been obvious to one ordinary skill in the art at the time the invention was made to have combined the teachings of applicant's admission of prior art and Klein" and that "[O]ne ordinary skill in the art would have been motivated to set initial values for initialization of the CPU based on received initialization data from North Bridge, since that would remove a number of strapping and jumping for setting the initialization data."

Applicants respectfully disagree for the following reasons.

Claim 33 now recites:

The method of claim 12, wherein step (d) comprises:

receiving the initialization data sent from the south-bridge chip by the north-bridge chip,

sending an initiating signal to the central processor unit to set initial values for initialization of the central processor unit based on the received initialization data received by the north-bridge chip from the south-bridge chip, wherein **no random access memory is used to store said initialization data during step (d).**

Claim 34 now recites:

The apparatus according to claim 20, wherein in response to the initialization data sent from the south-bridge chip, **the north-bridge chip sends an initiating signal to the central processor unit to set the initial values for initialization of the central**

processor unit based on the received initialization data from the south-bridge chip in order to activate the central processor unit without using any random access memory to store the initialization data.

It is respectfully submitted that neither the AAPA nor Klein disclose or suggest the features recited in claim 33 or 34. Claims 12 and 20 include features similar to those recited in claim 1. Consistent with the above discussion as to the patentability of claims 1, 12, and 20, it is respectfully submitted that claims 12 and 20 are not rendered obvious by Klein and the AAPA. In rejecting claims 33 and 34, no convincing suggestion or motivation has been advanced as to why one of ordinary skill in the art at the time of the invention would have been motivated to modify or combine Klein with the AAPA so as to arrive at all features required by the rejected claims. In particular, the proposed combination, as for claims 33 and 34, fails to disclose or suggest that **no random access memory is used to store the initialization data during sending an initiating signal to the central processor to set the initial values for initialization of the central processor unit based on the received initialization data from the south-bridge chip** and **the initialization data is excluded from the BIOS and is used for initialization of the central processor unit, as similarly required by the claims rejected**. For at least this reason, it is respectfully submitted that claims 33 and 34 patently define over Klein in view of the AAPA, and that the rejection of these claims should be withdrawn.

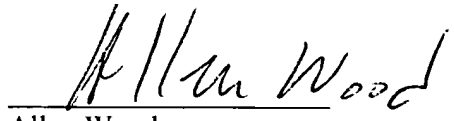
It is respectfully submitted that the rejections in the Office Action represent a classic example of impermissible hindsight reasoning. Moreover, the Office Action has pointed to ***no teaching within the prior art that relates the desirability of combining the selected features***. As discussed above, it is the prior art which must properly suggest the desirability of combining the particular elements, for it is axiomatic that all elements and features are taught somewhere in the

prior art. Thus, for at least these reasons, as a matter of law, the rejections of claims 33-34 are improper and should be withdrawn.

Conclusion

Based on the foregoing, it is submitted that this application is in condition for allowance. Notice of such action and the passing of this case to issue are therefore respectfully requested.

Respectfully submitted,



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